JSS Mahavidyapeetha

JSS Academy of Technical Education, Noida

Department of Electronics & Communication Engineering.

FACULTY PROFILE

1. Personal Details

NAME	**Dr. RASHIKA ANURAG**
DEPARTMENT	ELECTRONICS & COMMUNICATION ENGINEERING
DESIGNATION	ASSISTANT PROFESSOR-3
PHONE	9871644060
EMAIL ID	raashika@jssaten.ac.in
Date of Joining (JSSATEN)	19/4/2005

2. Experience

Total Experience in Years: 33	Teaching: 27 years	Industry: 01 Years	Research: 05 Years

3. Qualifications

COURSES	SPECIALIZATION	Year of Award	INSTITUTION	UNIVERSITY
B. Tech.	Electronics and Communication Engineering.	1990	J K Istitute	Allahabad University
M. E.	Electronics And Control	1993	Birla Institute of Tech. and Science. Pilani	Bits Pilani
Ph.D.	Analog VLSI	2018	Banasthali University	Banasthali University
Post Doc.	-	-	-	-

4. Research & Publications

Papers Published in Web of Science indexed Journals	International: 00	National: 00
Papers Published in SCOPUS indexed Journals	International: 01	National: 00

Papers Published in other Journals	International: 04	National: 00
Papers Presented in Conferences / Symposium	International: 01	National: 00
Books / Book chapters Published	Name of the book: NIL Publisher: Year of Publication:	

5. Research Guidance

PhD Guide? Give field & University	No	NA
Ph.D.s / Projects Guided	Ph.D. Awarded: NA Guiding: NIL	Projects at Master's Level: 4 Projects at Bachelor's Level: 35

6. Grants

i. Funds Received (Projects)

Project Name	Grant Amount	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	-	-	-	-

ii. Patents

Sl. No.	Title Details	Details of award of patent / Filed
-	-	-

iii. Consultancy

Title of the work	Amount in Rs.	Date of receiving the Grant	Duration	Grant issuing authority/ Body / Organization
-	-	-	-	-

7. Awards Received

Awards "Best Paper Award"	**"OTRA based shadow filters"** International Conference, 12th IEEE India, International Conference Electronics, Energy, Environment, Communication, Computer, and Control Dec 2015.

8. Publications

i. International Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
1	A Class of Differentiator – based Multifunction Biquad Filters Using OTRAs	Neeta Pandey , Rajeshwari Pandey,**RashikaAnuragand** Ritu Vijay	Advance in Electrical and Electronic Engineering	Volume 18, No. 1 (2020) March	Scopus	0.92	VSB Technical University of Ostrava
2	All Pass Network Based MSO using OTRA	Rajeshwari Pandey, Neeta Pandey, RomitaMullick, SarjanaYadav and **RashikaAnurag**	Advances in Electronics	volume 2015, Article ID 382360, 7 pages http://doi.org/10.1155/2015/382360	Non-Scopus	0.59	Hindawi Publishing Corporation
3	OTRA Based Precision Rectifier	**RashikaAnurag,** Neeta Pandey, Rajeshwari Pandey and Ritu Vijay	Journal on Electronics Engineering	January 2015, 6(1) :21 DOI:10.26634/jele.6.1.3682	Non-Scopus	1.130	I-manager's
4	LC-ladder filter systematic implementation by OTRA	SumanKumari, Stuti Gupta, Neeta Pandey , Rajeshwari Pandey and **RashikaAnurag**	Engineering Science and Technology, an International Journal	19 (2016) 1808–1814 www.elsevier.com/locate/jestch	Scopus	4.30	Elsevier
5	Voltage Mode Second Order Notch/ All – Pass Filter Realization Using OTRA	**RashikaAnurag,** Neeta Pandey, Chandra Rohan and Rajeshwari Pandey	Journal on Electronics Engineering	vol. 6, No. 22,DOI: 10.26634/jele.6.2.3763	Non-Scopus	1.130	I-manager's

ii. National Journals

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Journal	Volume No. Issue No. Year	WOS / Scopus / Both	Impact Factor	Publisher
-	-	-	-	-	-	-	-

iii. Conferences

Sl. No.	Title of the paper	Name(s) of Author(s)	Name of the Conference	Volume No. Issue No. Year	WOS / Scopus	Impact Factor	Publisher
1	"OTRA based shadow filters"	Dr. RashikaAnurag	International Conference	12th IEEE India, International Conference Electronics, Energy, Environment, Communication, Computer, and Control Dec 2015.2015)	-	-	IEEE

iv. Workshops /Conferences Attended

Sl. No.	Name of the workshop / Conference	Organizer	Date
1	Workshop on WSN using Netsim.	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	28th to 29th Oct 2015.
2	One week faculty development programme on "Wireless Networks" held at JSSATE, NOIDA . This programme will be in ICT mode with NITTTR, Chandigarh.	JSSATE, Noida conducted by Department of Electronics &Communication Engineering.	May 02 to May 06, 2016.
3	Three days workshop on "Linear Integrated Circuits - a system approach".	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	08/09/2016 to 10/09/2016
4	Faculty development program on "VLSI, Signal Processing for Communication".	ABES Engineering College, Ghaziabad .	12-16 June 2017
5	Attended FDP on Industrial Automation with Robotics & 3D Printer.	JSSATE, Noida conducted by Department of	4-06-2018 to 09-06-2018

		Electronics & Communication Engineering.	
6	Three days workshop on "Analog Applications".	ABESIT, Ghaziabad.	18th August to 20th August 2018
7	Six days FDP on "Analog Integrated Circuit Design Using Cadence Analog Design Flow.	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	27th August - 01 September 2018
8	Workshop on Human Values & Professional Ethics (UHVPE)	KIET, Ghaziabad	26/12/2019 to 02/01/2020

v. Workshops / Conference (Organized)

Sl. No.	Name of the workshop / Conference	Organized by	Date	Role
1	Analog System Design and IOT Application	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	21/08/2015	Deputy Coordinator
2	TI Webinar Series	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	9/04/2016, 21/04/2016 & 22/04/2016	Deputy Coordinator
3	Analog/Embedded Technologies	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	05/09/2016 to 10/09/2016	Deputy Coordinator
4	Analog Integrated Circuit Design Using Cadence Analog Design Flow	JSSATE, Noida conducted by Department of Electronics & Communication Engineering.	27/08/2018 to 01/09/2018	Deputy Coordinator

vi. Conference Attended (those sponsored by AICTE / ISTE/IETE/TEQIP or any other sponsoring body)

Sl. No.	Name of the workshop / Conference	Organizer	Date
1	Analog Integrated Circuit Design Using Cadence Analog Design Flow	JSSATE, Noida conducted by Department of Electronics & Communication Engineering	27/08/2018 to 01/09/2018

9. Details of NPTEL / COURSERA courses completed

Sl. No.	Name of the subject	Organized by	Date of completion / Award	Grade / Marks
-	-	-	-	-

10. Membership of Professional Bodies:

Nil

11. Any other information you will like to share about your professional experience

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